Decoupling Design through Parasitic Elements Analysis for Test Boards

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***Abstract*—In this paper, the implementation of the low power impedance through the power and ground analysis has been focused on the multilayer printed circuit board (PCB) to obtain the testability of the high speed memory devices, such as graphic DDR (GDDR), extreme data rate (XDR) RAM, and so on. The inductance between power and ground plane and the unexpected resonance at the frequency near a board resonance can be analyzed with the time domain reflectometry (TDR), vector network analyzer (VNA), and the computer aided software.**

Keywords - power impedance, inductance, high speed, unexpected resonance, through via, EMI

I. INTRODUCTION

As the clock and IO speeds of the current memory devices increase, it becomes very important to solve the signal integrity (SI) and electromagnetic interference (EMI) problems, which can be generated by the high frequency noise on the power plane in the multilayer PCBs. Generally, the decoupling capacitors between the power and ground plane are accomplished to mitigate the power noise from DC to the board resonant frequency [1]. Above this frequency, the decoupling capacitors have typically high impedance by the inductance of the through via and solder pad length. Therefore, the impedance characteristics between the power and ground plane is more important than the impedance of the decoupling capacitors with the increasing frequency. It is a common idea that the parasitic inductance related with the through via and solder pad on the top or bottom layer generally makes the decoupling capacitors ineffectively at the high frequency. In order to minimize the parasitic inductance on the thick board, the location of the decoupling capacitors is important, since the total distance between the power and ground plane will be determine the inductance curve of the capacitor [2].

Another consideration is the appearance of the unexpected resonance on the power and ground plane in the multilayer PCB. As the unexpected resonance at the frequency near board resonance is generated, the performance of the total system can be degraded on the view of the signal integrity and EMI noise. Therefore, it would be required to analyze the cause of the unexpected resonance and reconstruct by the modeling circuit to improve the testability of the high speed memory devices. In this paper, the implementation of the low power impedance by the power and ground resonance analysis has been focused on the multilayer printed circuit board (PCB) to test the high speed memory devices, such as graphic DDR (GDDR), extreme data rate (XDR) RAM, and so on. However, the inductance associated by the through via and the unexpected resonance can cause a rapid drop in the voltage in the high speed memory test field. Therefore, it presents the power design with the low impedance up to the high frequency (1 GHz) with a modeling approach to improve the signal quality and EMI characteristics. This paper shows the improvement to the decoupling performance at high frequencies with the analysis for the inductance of through via and unexpected resonance.

II. MODELING APPROACH

A. Power impedance by the parasitic inductances

The power impedance between power and ground plane would be determined by the physical layout size and PCB layer stack-up methodology. However, the capacitance created by this pair alone is not adequate to overcome the rapid current response of the high speed digital devices. Therefore, the discrete decoupling capacitors are required to supply the most of charges and minimize the power impedance at any frequency band where the impedance of the decoupling capacitor is lower than that of the power and ground plane. The increase of the equivalent series resistance (ESR) and equivalent series inductance (ESL) for the decoupling capacitor degrades the effective frequency bandwidth which makes to cope with the rapid current variation due to the simultaneous switching noise (SSN) of the high speed devices. Therefore, the use of the decoupling capacitor at the top or bottom layer traditionally placed adjacent to individual devices to sufficiently obtain the effective bandwidth of the capacitor. Actually, the self power impedance of the power and ground plane is a very important design factor to complement the ineffective region not to be covered by the decoupling capacitor. In order to obtain the effective region up to the high frequency, it is necessary to analyze the inductance added on the decoupling capacitor and the self resonance frequency related with the power and ground plane [3].

The power impedance distribution of the bare PCB can be analyzed by using the 3D EM-simulation or the simple RLC series circuit, as shown in Fig. 1.

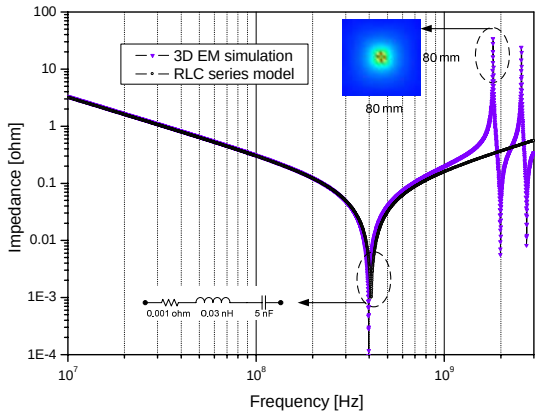

Figure 1. Modeled power impedance distribution.

It was a three layer PCB with the strip line structure and the dielectric layer was a PPE material with a dielectric constant of 3.5, loss tangent of 0.002 and thickness of 0.1 mm. Since the inductance (L_{pp}) and power impedance associated with the power and ground plane has a small value beyond self resonance frequency, 400MHz, the external inductance by the through via (L_{icvia}/L_{gvia}) connecting the decoupling capacitor and the distance (L_{dist}) between the decoupling solder pad and the power pin of IC can not be neglected to sufficiently obtain the effective bandwidth of the capacitor, as shown in Fig. 2. The total inductance (L_{tot}) between the power pin of IC and the power plane can be represented as

$$L_{tot} = L_{pvia} + L_{gvia} + L_{icvia} + L_{dist} + L_{pp} . \quad (1)$$

As the impedance of the power plane only with L_{pvia} and L_{gvia} will be simulated on port 1 (P1), the maximum available inductance of decoupling capacitor can be calculated. Fig. 3 shows a plot of the impedance of a power plane connected with via which has a diameter of 0.25 mm. At frequency greater than 30 MHz, the inductance between the power and bottom plane is approximately 7.4 nH alone. It means that the charge of power plane can not be normally supplied into IC due to the increased inductance by via. In order to obtain the lower impedance at the high frequency, the IC can be placed on the top plane which is the nearest to the power plane [4].

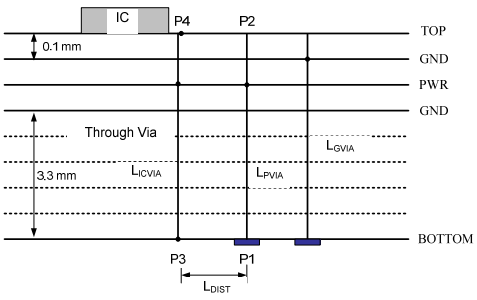

Figure 2. Various inductance model of a multilayer PCB.

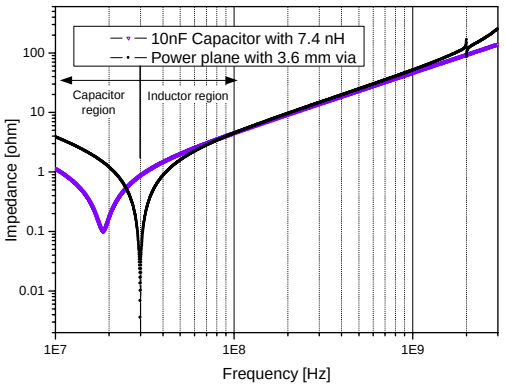

Figure 3. Impedance of a power plane connected with a via.

B. *Unexpected resonance analysis*

The capacitors placed on the bottom plane is electrically connected to the power and top plane through a via which has a length of 3.6 mm between the top and bottom plane and also makes some inductance. As a matter of fact, the parasitic inductance associated with the interconnection of a decoupling capacitor can be determined from the physical size of the plane and via. Since the capacitance and inductance of the power plane can be easily modeled and calculated from the resonant frequency, the inductance's value of a via can be also obtained [5]. Therefore, the decoupling capacitor attached on the bottom plane has been limited to operate as a capacitor above the resonant frequency due to the parasitic inductance by a via. At the frequency near the resonant frequency between the power and bottom plane, the unexpected resonance has been simultaneously generated by the decoupling capacitors which are placed on the bottom plane and not dramatically reduced by any capacitors [6].

The equivalent circuit of the power and ground plane will be connected with a parallel circuit, $Z_{in\text{-}total}$, the series resonant circuits of the bare board, $Z_{in\text{-}bare}$, and decoupling capacitor, $Z_{in\text{-}cap}$, which include the inductance of a via, as shown in below equations.

$$Z_{in-bare,\,in-cap} = R_{b,c} + j\omega L_{b,c} + j\omega L_{via1,2} - j \cdot \frac{1}{\omega C_{b,c}} . \quad (2)$$

$$Z_{in-total} = \frac{1}{R_{tot}} + j\omega C_{tot} + j \cdot \frac{1}{\omega L_{tot}} . \quad (3)$$

The parallel lumped element circuit model of the power impedance on the multilayer PCB consists with the series RLC model of the bare, decoupling capacitor, and the inductance of a via, as shown in Fig. 4. The combination of the RLC series and parallel resonant circuits also make the unexpected resonance with the high power impedance at the particular frequency, as shown in Fig. 5.

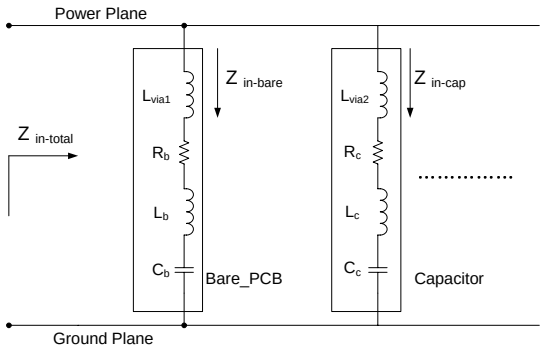

Figure 4. Equivalent circuit model for the power impedance.

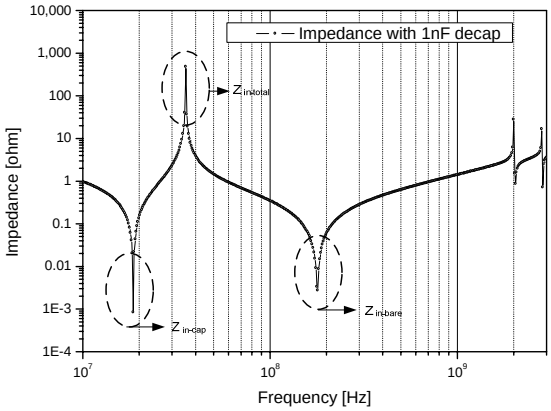

Figure 5. Impedance distribution with the series and parallel circuit.

As this modeled circuit indicates, the inductance on a PCB will be no longer ignored to accomplish the effectiveness of the decoupling capacitors on the wide frequency bandwidth [6].

III. Test Board Measurement

A test board was built to confirm the correlation between the power impedance model and the parasitic elements. It was a multilayer PCB with the top layer to measure the S-parameter and its bottom layer to solder the decoupling capacitors, as shown in Fig. 2. The board for the memory test was designed and fabricated specially for evaluating the inductance and unexpected resonance and confirming the equivalent model circuits. It was a 36 layer PCB with the strip line structure as a signal line and the plane structure as the power and ground. The dielectric was a PPE material of Kyocera Company with a dielectric constant of 3.5, loss tangent of 0.002 and thickness of 0.1 mm. The total thickness of a test board is about 3.8 mm. A vector network analyzer with the S-parameter test set was connected to the top plane through a 800μm pitch SG probe tip to measure the impedance of a inter-power plane. The power impedance of a PCB can be related to a one-port measurement on the power pin of IC. The input impedance can be directly calculated as using the S_{11} measured data. The capacitance and inductance of the through via and solder pad can be also evaluated and calculated by TDR.

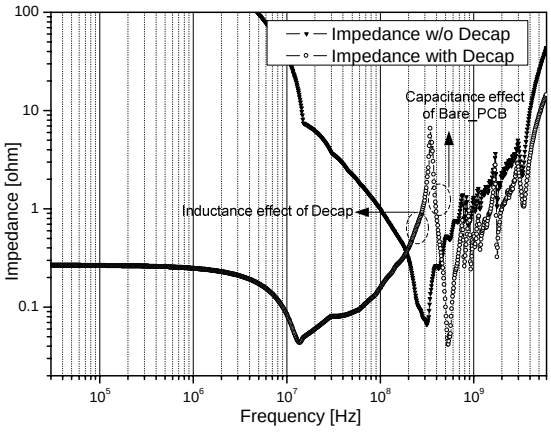

Figure 6. Measurement result with the unexpected resonant.

Fig. 6 shows the measurement result of the test board, which characterized the effect of the parasitic elements with the analysis of the series and parallel resonance generations between the power and ground plane on the multilayer PCB. It indicates that the inductance and capacitance effects generated by the decoupling and bare PCB has been represented through the unexpected resonance which makes a high impedance for the power and ground plane at the specific frequency.

In order to minimize the unexpected resonance, it has been designed the optimized test board through the via diameter, anti-pad size, capacitors' position, and so on. Using the optimized power and ground implementation, it can be obtained the test board with the lower power impedance within the broadband frequency, as shown in Fig. 7.

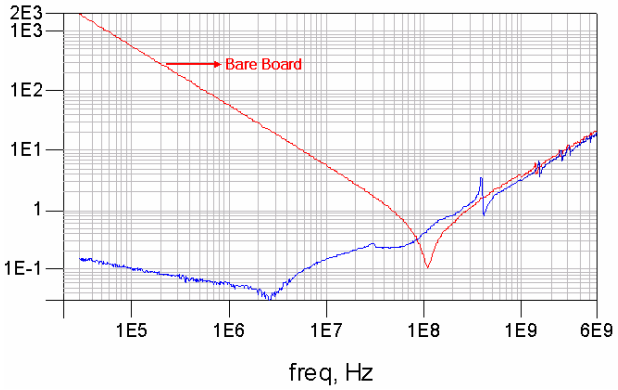

Figure 7. Measurement result with the unexpected resonant.

IV. Conclusions

The decoupling capacitor has some limitations to operate as a capacitor above the resonant frequency due to the parasitic inductance. In case of the thick multilayer PCB, the low power impedance is very difficult to construct only with the power plane structure and decoupling capacitors. In order to achieve the low power impedance, it is necessary to analyze the

impedance distribution through the RLC series and parallel resonant equivalent circuit which consists with the through via, decoupling capacitors, and physical size of the power plane on the multilayer PCBs. As a matter of fact, the construction of the test board with the low power impedance has been accomplished to normally operate the high speed memory devices, such as GDDR, XDR, and so on. Actually, the signal quality has been directly connected with the power integrity which would be determined by the power impedance on the designed frequency band. The extra inductance on the multilayer PCBs can cause a rapid drop in the voltage in the high speed memory test field.

With the analyzed power plane and calculated decoupling capacitors, the low power impedance can be dramatically achieved through some method, such as the stack-up structure of multilayer, the optimization between the dielectric constant of the substrates and physical size of the power planes, the diameter and count of a through via, and so on. This paper shows the improvement to the decoupling design at the designed high frequencies with the analysis for of through via and unexpected resonance.

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